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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10080831	FILING DATE 02/21/2002	CLASS 257	SUBCLASS 48	GAU 2844	EXAMINER <i>Edith Lee</i>
**APPLICANTS: Hino Yoshinori; Takeishi Naoei; 2815					
**CONTINUING DATA VERIFIED:					
** FOREIGN APPLICATIONS VERIFIED: JAPAN P 2001-053627 02/28/2001					
PG-PUB		DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>	
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no Verified and Acknowledged Examiners's initials				ATTORNEY DOCKET NO 10417-119001 / F51-143213	
TITLE : Semiconductor device and pattern layout method thereof					

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Assistant Examiner	Total Claims Print Claim for O.G.
ISSUE FEE		Primary Examiner	DRAWING
Amount Due	Date Paid		Sheets Drwg. Figs. Drwg. Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Applicant Examiner
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